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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/360,069	07/23/1999	PETER WOHL	SNSY-A1998-0	3639

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EXAMINER	
GARCIA OTERO, EDUARDO	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 05/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/360,069	WOHL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the c ver sheet with the c rrespondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 July 1999 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Examined

1. **Claims 1-36 have been submitted, examined, and rejected.**

Information Disclosure Statement—37 CFR 1.56 Duty to Disclose

2. 37 CFR 1.56 states "Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section". Please note that the following 7 documents (3 patents and 4 publications) have been identified by the Examiner as prior art, but were not disclosed by Applicant. Additionally, please note that Applicant Peter Wohl is the inventor, or co-inventor, or author, or co-author of all of these 7 documents.

   (a) Appenzeller, and Wohl US Patent 5,508,641

   (b) Pederson and Wohl US Patent 5,668,492

   (c) Eire and Graf and Wohl US Patent 5,796,990

   (d) "Using Verilog simulation libraries for ATPG", Wohl et al, Test Conference, 1999. Proceedings. International, 1999 Pages 1011-1020

   (e) "Defining ATPG rules checking in STIL", Wohl et al, Test Conference, 1998. Proceedings., International, 1998 Pages 971-979

   (f) "Using ATPG for clock rules checking in complex scan designs", Wohl et al, VLSI Test Symposium, 1997., 15th IEEE, 1997 Pages 130-136

(g) "Test generation for ultra-large circuits using ATPG constraints and test pattern templates", Wohl et al, Test Conference, 1996. Proceedings., International, 1996 Pages 13-20.

Drawings-draftperson objection

3. **This application has been filed with informal drawings** which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed. Specifically, see the enclosed Form 948, Notice of Draftperson's Drawing Patent Review which objects to the drawings.

Drawings-replete with prior art

4. **The drawings are replete with figures that should be designated by a legend such as --Prior Art--** because only that which is old is illustrated. See MPEP § 608.02(g). The drawings should be revised carefully in order to comply with MPEP § 608.02(g). Specifically, some examples are: FIG 2 is "an exemplary general purpose computer system" according to Page 12 line 22, and FIG 5 is an exemplary simulation model of a ROM. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Drawings-other objections

5. FIG 1 should have an arrow pointing from element 11 to element 15 because "manual re-coding process 15 must be performed by the designers to translate the simulation library 11 into the test library 12" according to Page 2 line 25.

Specification-objections-informalities

6. **The disclosure is objected to because of the following informalities.** Appropriate correction is required.

7. Page 8 line 19 states "Figure 4 is a formal description of a memory port" and contradicts Page 16 line 8 which states "Figure 4 illustrates **simplified** formal description 400 of a memory port".

8. Page 15 line 26 states "co-pending US patent application serial no., 09/052,998". Said application was **issued** on Nov. 14, 2000 as US patent 6,148,436.

Claim Rejections - 35 USC § 112- first paragraph- enablement

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. **Claims 1-3, 12, 13-15, 24, 25-27, and 36 are rejected under 35 U.S.C. 112, first paragraph,** as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

11. **Claim 1 states "predefined subset".** The specification does not adequately describe "predefined subset".

12. **Claim 2 states "excludes timing information". The** specification des not adequately describe "excludes timing information".

13. **Claim 3 states "excludes physical layout information".** The specification does not adequately describe "excludes physical layout information".

14. **Claim 12 states "displaying a graphical representation of said primitives".** The specification does not adequately describe "displaying a graphical representation".

15. **Claims 13-15 and 24 are "computer readable medium"** claim with the same limitations as Claims 1-3 and 12, and therefore are rejected for the same reasons.

16. **Claims 25-27 and 36 are "computer controlled electronic design automation systems"** (apparatus) claims with the same limitations as Claims 1-3 and 12, and therefore are rejected for the same reasons.

Claim Rejections - 35 USC § 112-Second Paragraph-indefinite claims

17. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

18. **Claims 3, 15, and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

19. **Claim 3 is rejected because the words "excludes physical layout information" render the claim indefinite.** Specifically, Claim 1 is indefinite because it is unclear how a simplified behavioral model can exist without implicit physical layout information.

20. **Claim 15 is a "computer readable medium"** claim with the same limitations as Claim 3, and therefore are rejected for the same reasons.

21. **Claims 27 is a "computer controlled electronic design automation systems"** (apparatus) claim with the same limitations as Claim 3, and therefore are rejected for the same reasons.

No Prior Art Examination - Indefinite Claims - In re Steele

22. **Claims 3, 15, and 27 are so indefinite that no prior art examination is feasible.** Specifically, the Examiner should not rely "on what at best are speculative assumptions as to the meaning of the claims", and should not base "a rejection under 35 U.S.C. 103 thereon...[when] the claims do not particularly point out and distinctly claim the invention as required by 35 U.S.C. 112." In re Steele , 305 F.2d 859, 134 USPQ 292, 295 (CCPA 1962). Also see In re Citron, 45 CCPA 773, 251 F.2d 619, 116 USPQ 409.

23. Note that Claims 3, 15, and 27 have been rejected under 35 USC 101 for lack of utility, and 25 USC 112 First Paragraph for lack of enablement, and further rejected under 112 Second Paragraph for indefinite claims. The Examiner believes that it would be counter-productive to make speculative assumptions about the meanings of Claims 3, 15, and 27 for the purpose of examination against prior art. These claims will be examined against prior art only after such an examination becomes feasible.

Claim Rejections - 35 USC § 102(b)

24. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

25. A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

26. Claims 1, 4-12, 13, 16-24, 25, and 28-36 are rejected under 35 U.S.C. 102(b).

27. **Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Beausang US Patent 5,696,771.** Claim 1 is an independent claim with three limitations.

28. "**simulation model**" is disclosed by Beausang '771 at FIG 8 element 605 "HDL DESCRIPTION".

29. "**generating a simplified behavioral model**" is disclosed by Beausang '771 at FIG 8 element 645 "CONSTRAINT DRIVEN SCAN INSERTION".

30. "**plurality of ATPG memory primitives**" is disclosed by Beausang '771 at FIG 8 element 655 "ATPG AND FORMAT", and alternately disclosed at Column 14 line 40 "logical primitives".

31. **Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Beausang US Patent 5,696,771.** Claim 4 depends from Claim 1, and has one additional limitation, thus is rejected for the same reasons plus these additional reasons.

32. "plurality of ATPG memory primitives each represents a functionality" is disclosed by Beausang '771 at Column 14 line 40 "logical primitives".

33. **Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Beausang US Patent 5,696,771.** Claim 5 depends from Claim 1, and has five additional limitation, thus is rejected for the same reasons plus these additional reasons.

34. "**memory primitive**", "**address bus primitive**", "**data bus primitive**", "**read port primitive**", and "**plurality of macro output primitives**" are disclosed by Beausang '771 at Column 14 line 40 "logical primitives".

35. **Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Beausang US Patent 5,696,771.** Claim 5 depends from Claim 4, and has five additional limitation, thus is rejected for the same reasons plus these additional reasons.

36. **"address bus primitive", "memory primitive for coupling", "data bus primitive for coupling", "read port primitive for coupling", and "plurality of macro output primitives for coupling"** are disclosed by Beausang '771 at Column 14 line 40 "logical primitives".

37. **Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Beausang US Patent 5,696,771.** Claim 7 depends from Claim 4, and has three additional limitation, thus is rejected for the same reasons plus these additional reasons.

38. **"memory primitive", "compare port primitive" and "plurality of macro output primitives"** are disclosed by Beausang '771 at Column 14 line 40 "logical primitives".

39. **Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Beausang US Patent 5,696,771.** Claim 8 depends from Claim 4, and has three additional limitation, thus is rejected for the same reasons plus these additional reasons.

40. **"memory primitive", "compare port primitive for coupling to receive...comparing said first data and said second data" and "plurality of macro output primitives"** are disclosed by Beausang '771 at Column 14 line 40 "logical primitives".

41. **Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Beausang US Patent 5,696,771.** Claim 9 depends from Claim 1, and has one additional limitation, thus is rejected for the same reasons plus these additional reasons.

42. **"verifying functional equivalence between said simplified behavioral model and said simulation model by applying both models to a behavioral hardware description language simulator"** is disclosed by Beausang '771 at FIG 8 element 660 "TEST

VECTORS" and alternately disclosed at FIG 9 element 790 "VERIFY DESIGN TO HDL".

43. **Claim 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Beausang US Patent 5,696,771.** Claim 10 depends from Claim 1, and has one additional limitation, thus is rejected for the same reasons plus these additional reasons.

44. **"behavioral description language is Verilog"** is inherently disclosed Beausang '771 at FIG 8 element 605 "HDL DESCRIPTION" because Verilog is one of the two most common HDL languages (Verilog and VHDL).

45. **Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Beausang US Patent 5,696,771.** Claim 11 depends from Claim 1, and has one additional limitation, thus is rejected for the same reasons plus these additional reasons.

46. **"behavioral description language is VHDL"** is inherently disclosed Beausang '771 at FIG 8 element 605 "HDL DESCRIPTION" because VHDL is one of the two most common HDL languages (Verilog and VHDL).

47. **Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Beausang US Patent 5,696,771.** Claim 12 depends from Claim 1, and has one additional limitation, thus is rejected for the same reasons plus these additional reasons.

48. **"displaying a graphical representation of said primitives"** is inherently disclosed at Column 14 line 40 "logical primitives".

49. **Claims 13 and 16-24 are "computer readable medium" claims** with the same limitations as Claims 1 and 4-12, and therefore are rejected for the same reasons.

50. **Claims 25 and 28-36 are "computer controlled electronic design automation systems"** (apparatus) claims with the same limitations as Claims 2 and 3, and therefore are rejected for the same reasons.

Claim Rejections - 35 USC § 103

51. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

52. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

53. **Claims 2, 14, and 26 are rejected under 35 U.S.C. 103(a).**

54. **Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang US Patent 5,696,771 in view of Wohl and Waicukauski, "Using Verilog Simulation Libraries for ATPG".** Claim 2 depends from Claim 1, with one additional limitation, thus is rejected for the same reason plus these additional reasons.

55. Beausang '771 discloses all three limitations from Claim 1 (see above 102(b) rejection).

56. Beausang '771 does not expressly disclose "excludes timing information".

57. **"excludes timing information"** is disclosed by Wohl and Waicukauski at Page 1011 second full paragraph "The test library, by contrast, is purely structural, optimized for ATPG and has no timing". The Examiner notes that the present application consists of a different inventive entity (Wohl and Waicukauski and Hunkler) than that of "Using Verilog Simulation Libraries for ATPG" (Wohl and Waicukauski) and therefore constitutes 102(a) type prior art that may be used in a 103(a) rejection. Additionally, note that the MPEP 706.02(k) exclusion of 102(e) prior art assigned to the same person does not apply because: this is 102(a) type prior art, and also because this application was filed before November 29, 1999 (on July 23, 1999). Also note that 35 USC 103(c) does not apply.

58. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Wohl et al ("Using Verilog Simulation...") to modify Beausung '771. One of ordinary skill in the art would have been motivated to do this "to minimize or eliminate the engineering effort in creating a test library" according to Wohl et al ("Using Verilog Simulation...") Page 1011 third full paragraph.

59. **Claim 14 is "computer readable medium"** claim with the same limitations as Claim 2, and therefore is rejected for the same reasons.

60. **Claim 26 is "computer controlled electronic design automation systems"** (apparatus) claims with the same limitations as Claims 2, and therefore is rejected for the same reasons.

Conclusion

61. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 7:00 PM.

62. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:

63. (703) 746-7238 --- for communications after a Final Rejection has been made;

64. (703) 746-7239 --- for other official communications; and

65. (703) 746-7240 --- for non-official or draft communications.

66. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * * *

Eduardo Garcia-Otero
Examiner

William Thomson
Examiner